Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (currently amended) A power semiconductor device, comprising:

a substrate having an upper surface and a lower surface, the substrate having a trench;

first and second doped regions provided proximate the upper surface of the substrate;

a first source region provided within the first doped region;

a second source region provided within the second doped region; and

a gate provided between the first and second source regions, the gate including a first portion extending ~~downward into~~ laterally within the trench, wherein a depth of the trench is no more than a depth of the first doped region,

wherein the gate has a lateral extension and a vertical extension, the lateral extension being substantially greater than the vertical extension to reduce the curvature of equi-potential lines that are defined below the gate and the first and second dope regions.

2. (original) The power device of claim 1, further comprising:

a drain region provided proximate the lower surface of the substrate.

3. (original) The power device of claim 2, wherein the gate further comprises a second portion provided overlying the substrate and extending toward the first source region.

4. (original) The power device of claim 3, wherein the trench has smooth, continuous sidewalls formed using a deep oxidation process.

5. (original) The power device of claim 1, wherein a length of the first portion of the gate is greater than the depth of the trench.

6. (canceled).

7. (original) The power device of claim 1, wherein a ratio of a length of the first portion of the gate to the depth of the trench is at least 2.5:1.

8. (original) The power device of claim 1, wherein the depth of the first doped region is no more than about 5 micron.

9. (original) The power device of claim 8, wherein the depth of the trench is no more than about 2.5 micron.

10. (currently amended) The power device of claim 1, wherein the first portion ~~of the gate includes a planar portion that~~ is substantially parallel to the upper surface of the substrate.

11. (currently amended) The power device of claim 10, wherein the ~~planar~~ first portion is longer than about 1 micron.

12. (currently amended) The power device of claim 10, wherein the ~~planar~~ first portion is longer than about 2 micron.

13. (currently amended) The power device of claim 10, wherein the ~~planar~~ first portion is longer than about 3 micron.

14. (currently amended) The power device of claim 10, wherein the ~~planar~~ first portion is longer than about 4 micron.

15. (original) The power device of claim 14, wherein the device is an insulated bipolar gate transistor or a power MOSFET.

16. (currently amended) A power semiconductor device, comprising:

a substrate having an upper surface and a lower surface, the substrate having a trench;

a first doped region provided proximate the upper surface of the substrate;

a first source region provided within the first doped region; and

a gate provided adjacent the first source region, the gate including a first portion provided within the trench, wherein a depth of the trench is no more than a depth of the first doped region, the gate having a lateral extension and a vertical extension,

wherein the lateral extension of the gate is substantially greater than the vertical extension of the gate.

17. (currently amended) The power device of claim 16, further including:

a drain region provided proximate the lower surface of the substrate, wherein the lateral extension of the gate is at least 2.5 times greater than the vertical extension of the gate.

18. (original) The power device of claim 17, wherein the first portion of the gate is substantially parallel to the upper surface of the substrate and is longer than 2 micron.

19. (currently amended) A power semiconductor device, comprising:

a substrate having a first surface and a second surface, the substrate having a trench having a first depth;

a doped region provided proximate the first surface of the substrate and having a second depth;

a source region provided within the ~~first~~ doped region and proximate the first surface; and

a gate provided adjacent the source region, the gate including a first portion provided within the trench and a second portion provide outside of the trench, the first portion having a length that is greater than the first depth of the trench,

wherein the first portion includes a lateral extension and that is parallel to the first and second surface of the substrate,

wherein the lateral extension of the first portion is at least 2.5 times greater than the first depth of the trench.

20. (original) The power device of claim 19, wherein the first depth of the trench is no more than the second depth of the doped region, the device further comprising:

a drain region provided proximate the second surface of the substrate.

21. (original) The power device of claim 20, wherein the first portion is substantially planar and is longer than 2 micron.

22. (currently amended) A method for fabricating a power semiconductor device, comprising:

forming a shallow trench on a substrate having a first surface and a second surface, the shallow trench having a first depth and a width, the width of the shallow trench being greater than the first depth of the shallow trench;

forming a doped region provided proximate the first surface of the substrate and having a second depth;

forming a source region provided within the ~~first~~ doped region and proximate the first surface; and

forming a gate structure provided adjacent the source region, the gate structure including a first portion provided within the shallow trench and a second portion provide outside of the trench,

wherein the first portion includes a lateral extension and that is parallel to the first and second surface of the substrate,

wherein the lateral extension of the first portion is at least 2.5 times greater than the first depth of the shallow trench.

23. (original) The method of claim 22, wherein forming the shallow trench includes:

etching the substrate to form an intermediate trench having a third depth that is less than the first depth;

forming a first oxide layer within the intermediate layer; and

removing the oxide layer formed within the intermediate trench, wherein a resulting trench from the removal of the oxide layer has a fourth depth that is greater than the third depth..

24. (original) The method of claim 23, wherein an isolation trench is formed in another location on the substrate during the etching step, wherein a second oxide layer is formed within the isolation structure at the same time the first oxide layer is formed within the intermediate trench, the first oxide layer being further processed to be an isolation structure.

25-27 (canceled).

28. (new) A method for fabricating a power semiconductor device, comprising:

forming a shallow trench on a substrate having a first surface and a second surface, the shallow trench having a first depth and a width, the width of the shallow trench being greater than the first depth of the shallow trench;

forming a doped region provided proximate the first surface of the substrate and having a second depth;

forming a source region provided within the first doped region and proximate the first surface; and

forming a gate structure provided adjacent the source region, the gate structure including a first portion provided within the shallow trench and a second portion provide outside of the trench,

wherein forming the shallow trench includes:

etching the substrate to form an intermediate trench having a third depth that is less than the first depth;

forming a first oxide layer within the intermediate layer; and

removing the oxide layer formed within the intermediate trench, wherein a resulting trench from the removal of the oxide layer has a fourth depth that is greater than the third depth..

29. (new) The method of claim 28, wherein an isolation trench is formed in another location on the substrate during the etching step, wherein a second oxide layer is formed within the isolation structure at the same time the first oxide layer is formed within the intermediate trench, the first oxide layer being further processed to be an isolation structure.

30. (new) The power device of claim 1, wherein the gate is formed by etching the substrate to form an intermediate trench having a third depth that is less than the depth of the trench; forming a first oxide layer within the intermediate layer; and removing the oxide layer formed within the intermediate trench, wherein a resulting trench from the removal of the oxide layer has a fourth depth that is greater than the third depth.